Listing Of Claims

1. (Original) A system for converting a hardware description from a file in a high level language (HLL) used for hardware description to a translated file in a lower level language (LLL) used for hardware testing comprising;

means for adapting statements in said HLL to LLL statements that can be translated directly into test vector data,

means for producing a translatable file containing all said adapted HLL statements and said HLL statements that translate directly,

means for translating said translatable file into said translated file so that all statements in said translated file are LLL statements,

means for producing a logical test vector from said translated file, and

means for formatting said logical test vector to fit into logical registers in a relevant test device through a test input means of known configuration, thus producing a formatted test vector.

2 (Currently Amended) The system of claim 1 wherein said HLL is ~~Tel~~ TCL and said LLL is compatible with SVF.

3. (Original) The system of claim 1 wherein said formatting step depends upon a state item parameter file having information on the length and composition of the instruction registers associated with an interface to said test input means, what the data register instructions are, and an allowed functional clock state while executing interface register instructions on said instruction registers associated with said interface.

4. (Original) The system of claim 3 wherein the test input means interface is a TAP interface.

5. (Currently Amended) The system of claim 1 wherein said means for formatting comprises commercially available software ~~from JTag Tech~~ compliant with the IEEE JTAG standard.

6. (Original) A system for producing useable test vectors for testing particular circuits on particular boards of a multiprocessor computer system, said computer system having a support processor operating as a host computer for said system and wherein said support processor is also useful for producing said useable test vectors from high level language description files of said circuit boards comprising,

a support processor substantially equivalent to said support processor of said multiprocessor computer system, acting as a host computer for said multiprocessor system boards and for interpreting said high level language description files into new code of a lower level language, said new code being directly translatable into a test vector for a one of said particular circuits on said particular boards,

a simulation environment for use in generating new code from said interpreted code by capturing TAP, Clock and Control Commands on execution of said interpreted high level language description files,

an edge tester for receiving a test file list containing a test vector for testing said particular circuits on particular circuit boards, said edge tester having conversion software to convert a test file list into an appropriately formatted test vector for use through a specifically formatted interface in a connector for connecting a one of said particular boards to said edge tester.

7. (Currently Amended) The system of claim ~~5~~ 6 wherein said conversion software comprises commercially available software.

8. (Currently Amended) The system of claim 7 wherein said commercially available software ~~is available from JTag Tech~~ complies with the IEEE JTAG standard.

9. (Original) A system for converting a hardware circuit description for a hardware

circuit in a designer created file in a high level language (HLL) useful for describing hardware circuits, into a translated file in a lower level language (LLL) useful for hardware testing comprising;

a first conversion translator program for determining which statements in said designer created file will not convert correctly from said HLL into said LLL using an automatic conversion process, and which statements will; then for converting said statements that will not convert correctly into statements that will convert correctly, and for creating a file of translatable statements from both said converted statements and said statements that will convert,

a second conversion translator program for receiving from said first conversion translation program said file of translatable statements and for converting said file of translatable statements into a translated file, said translated file being of said LLL format,

a logical test vector production program for producing a logical test vector from said translated file, and

a formatting program for adapting said logical test vector into a test vector adapted to fit into logical registers in a test device constructed to conform to said hardware description in said designer created file, such that said test vector exercises circuits of interest when said test vector is delivered to said hardware.

10. (Original) The system of claim 9 wherein said logical test vector is created by said formatting program using a state item parameter file and a maintenance access generation file.

11. (Original) The system of claim 10, wherein said state item parameter file has a limited set of data regarding the hardware circuit, and the maintenance access generation file has a set of data regarding the interface from a tester to hardware circuitry under test.

12. (Currently Amended) The system of claim 5 wherein said HLL is ~~Tel~~ TCL and said LLL is SVF.

13. (Currently Amended) The system of claim ~~5~~ 9 wherein said logical test vector production program comprises a commercially available program.

14. (Original) A method for converting a hardware description from a file in a high level language (HLL) used for hardware description to a translated file in a lower level language (LLL) used for hardware testing comprising;

adapting statements in said HLL to statements that translate directly into said LLL and

producing a translatable file containing all said adapted HLL statements and said HLL statements that translate directly,

translating said translatable file into said translated file,

producing a logical test vector from said translated file, and

formatting said logical test vector to fit into logical registers in a relevant test device through a test input means of known configuration, thus producing a formatted test vector.

15. (Original) The method of claim 14 wherein said method of adapting comprises determining which HLL statements translate directly into LLL and which do not, then producing a set of statements that does translate directly into LLL

16. (Original) The method of claim 14 wherein said translating comprised forwarding said translatable file to a commercially available software program that translates the HLL file into a LLL file.

17. (Original) The method of claim 14 wherein said formatting said logical test vector to fit into physical equivalents of said logical registers through a said test input means of known configuration accounts for the physical configurations of an electronic system under test.

18. (Original) The method of claim 14 wherein said logical test vector is created by said formatting program using a state item parameter file and a maintenance access generation file.

19. (Original) The method of claim 14 further comprising creating a test vector from said logical test vector and exercising a circuit in a tester using said test vector.

20. (Original) The method of claim 19 further comprising producing an isolation file for isolating faults for use to examine fault results from said test vector.

21. (Original) The method of claim 20 wherein using said isolation file is consulted to produce data indicating which components of a unit under test are bad.